19-3848; Rev 1; 10/08

EVALUATION KIT AVAILABLE

155Mbps to 2.5Gbps Burst-Mode Laser Driver

General Description

The MAX3643 burst-mode laser driver provides bias and modulation current drive for PON burst-mode ONT applications. It is specifically designed for use with a low-cost external controller for the APC (and if desired, AMC) loop. A high-speed differential burst-enable input enables the driver to switch the laser from a dark (output off) condition to full on-condition in less than 2ns. When BEN is inactive, typical modulation and bias currents are 5µA each.

Laser modulation current can be set from 10mA to 85mA and bias current can be set from 1mA to 70mA using the MODSET and BIASSET inputs. A sample-and-hold circuit is provided to capture the monitor diode output during short PON bursts, if needed, and the BEN high-speed signal is mirrored on an LVCMOS output to be used by the controller operating the APC/AMC loop.

The MAX3643 burst-mode laser driver is packaged in a 4mm x 4mm, 24-pin thin QFN package. It operates from -40°C to +85°C.

Applications

A/B/GPON ONT Modules up to 2.5Gbps

1.25Gbps IEEE EPON ONT Modules

Features

- **10mA to 85mA Modulation Current**
- **1mA to 70mA Bias Current**
- **Monitor Diode Sample and Hold**
- **45ps Output Transition Time**
- **2ns Turn-On/-Off Time**
- **Reference Voltage Generator**
- **LVPECL High-Speed Inputs (Data, Burst Enable)**

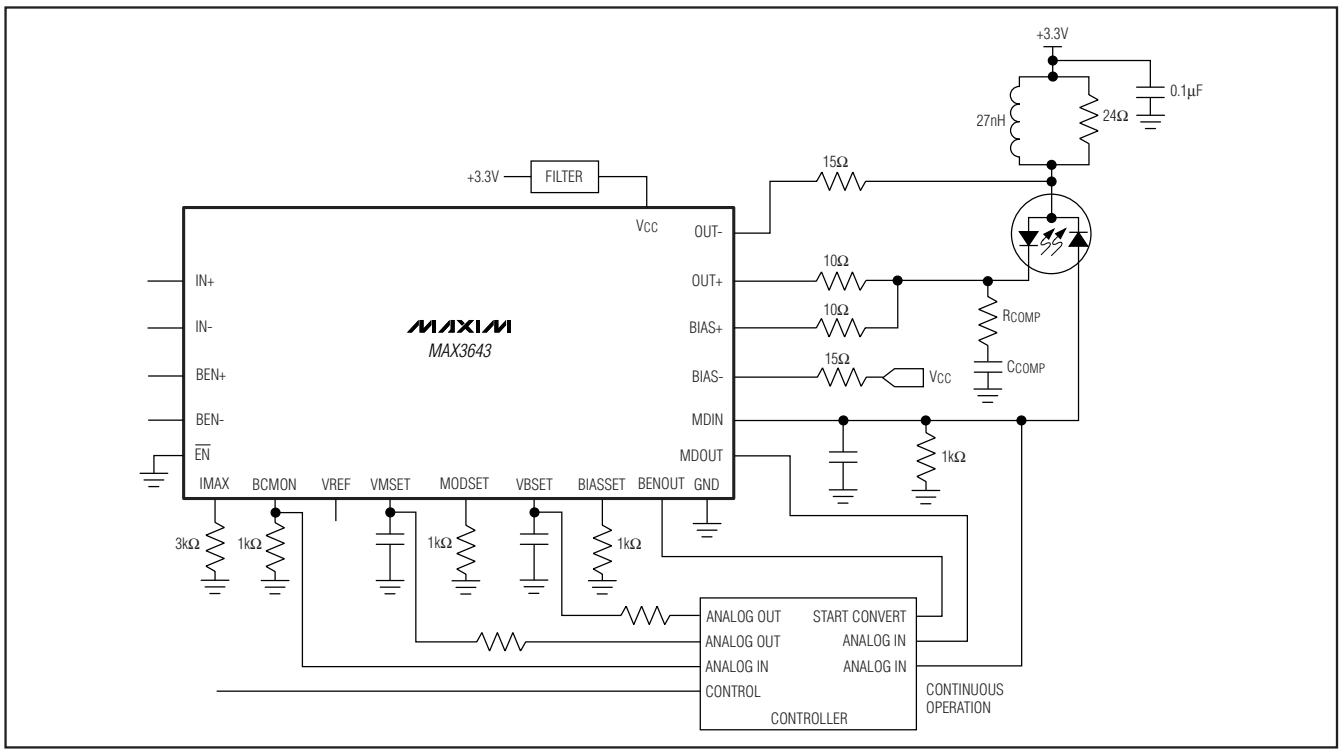
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3643ETG	-40°C to +85°C	24 TQFN-EP*
MAX3643ETG+	-40°C to +85°C	24 TQFN-EP*

+Denotes a lead-free/RoHS-compliant package.
**EP = Exposed paddle.*

Pin Configuration appears at end of data sheet.

Typical Application Circuit



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} .....-0.5V to +4.0V
Current into BIAS-, BIAS+, OUT-, OUT+ .....-20mA to +150mA
Voltage at VMSET, VBSET, IN+, IN-, BEN+, BEN-, $\overline{EN}$, MDIN, MDOUT, BENOUT, BIASMON .....-0.5V to (V_{CC} + 0.5V)
Voltage at MODSET, BIASSET, VREF, IMAX .....-0.5V to +3.0V
Voltage at OUT-, OUT+, BIAS-, BIAS+ .....+0.3V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
24-Pin TQFN, Multilayer Board
(derate 27.8mW/°C above +85°C).....1807mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Turn-On Time		10% to 90%	0.001		1000	ms
Ambient Temperature			-40		+85	°C
Data Rate					2500	Mbps
Voltage at VMSET, VBSET			0		1.4	V
Voltage at BIASMON			0		1.4	V
Voltage at MDIN			0		2.56	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, I_{BIAS} = 20mA, I_{MOD} = 30mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	Excluding laser bias and mode currents, max at I_{MOD} = 85mA, I_{BIAS} = 70mA		32	51	mA
I/O SPECIFICATIONS						
LVPECL Differential Input Voltage	V_{IN}	$V_{IN} = (V_{IN+}) - (V_{IN-})$	200		1600	mV_{P-P}
LVPECL Common-Mode Input Voltage	V_{CM}		V_{CC} - 1.49	V_{CC} - 1.32	V_{CC} - V_{IN} / 4	V
LVCMOS Output High Voltage		I_{OH} = -100µA	V_{CC} - 0.2			V
LVCMOS Output Low Voltage		I_{OL} = 100µA			0.2	V
BENOUT Propagation Delay	T_d	C_L = 20pF, from BEN zero crossing to 67% CMOS level		30		ns
LVCMOS Input Pullup Resistance			75			kΩ
LVCMOS Input Current		V_{IN} = 0V or V_{IN} = V_{CC}			50	µA
LVCMOS Input High Voltage			2.0		V_{CC}	V
LVCMOS Input Low Voltage			0.2		0.8	V
BIAS GENERATOR SPECIFICATIONS						
Bias Current Range	I_{BIAS}	V_{BIAS+}, V_{BIAS-} ≥ 0.6V	1		70	mA
Bias Current, Burst Off	$I_{BIAS, OFF}$	BEN = low or $\overline{EN}$ = high		5	50	µA
BIASSET Current Gain	G_{BIAS}	1mA ≤ I_{BIAS} < 2mA, VBSET = VREF		88		mA/mA
		2mA ≤ I_{BIAS} < 10mA, VBSET = VREF	70	88	110	
		10mA ≤ I_{BIAS} < 70mA, VBSET = VREF	82.5	88	94.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, I_{BIAS} = 20mA, I_{MOD} = 30mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIASSET Current Gain Stability		5mA ≤ I_{BIAS} ≤ 70mA (Note 13)	-4.4		+4.4	%
BIASSET Current Gain Linearity		5mA ≤ I_{BIAS} ≤ 70mA (Note 14)	-3.75		+3.75	%
Bias Current Overshoot		V_{CC} turn-on/-off < 1s			10	%
Bias Current Monitor Gain	G_{BSM}	2mA ≤ I_{BIAS} ≤ 70mA, VBSET = VREF	11	14	17	mA/A
Bias Current Monitor Gain Stability		1mA ≤ I_{BIAS} < 5mA		±4		%
		5mA ≤ I_{BIAS} ≤ 70mA	-5		+5	
BIASSET Resistor	R_{BIAS}		40	50	60	Ω
MODULATOR SPECIFICATIONS						
Modulation Current Range	I_{MOD}		10		85	mA
Modulation Current Off	$I_{MOD, OFF}$	BEN = low or $\overline{EN}$ = high or V_{IN} = low		5	120	µA
Instantaneous Voltage at OUT+		10mA ≤ I_{MOD} < 60mA	0.6			V
		60mA ≤ I_{MOD} ≤ 85mA	0.75			
MODSET Current Gain	G_{MOD}	10mA < I_{MOD} < 85mA, VMSET = VREF	82.5	88	94.5	mA/mA
MODSET Current Gain Stability		(Note 13)	-4.4		+4.4	%
MODSET Current Gain Linearity		(Note 14)	-2.2		+2.2	%
MODSET, BIASSET Gain Matching (Note 15)		$I_{BIASSET}$ = 0.15mA, I_{MODSET} = 0.7mA		0.5		%
		I_{MODSET} = $I_{BIASSET}$ = 0.15mA			1.7	
		I_{MODSET} = $I_{BIASSET}$ = 0.4mA			1	
		I_{MODSET} = $I_{BIASSET}$ = 0.55mA			1	
Modulation Current Rise Time	t_R	20% to 80%		45	85	ps
Modulation Current Fall Time	t_F	20% to 80%		45	85	ps
Deterministic Jitter		(Note 3)		17	45	ps_{P-P}
Random Jitter		(Note 4)		0.8	1.4	ps_{RMS}
MODSET Resistor	R_{MOD}		40	50	60	Ω
MODSET, BIASSET OPERATIONAL AMPLIFIER SPECIFICATIONS						
MODSET, BIASSET Voltage Range			0.005		1.4	V
Voltage Error		(Note 5)			±5	mV
Input Leakage		VMSET and VBSET pins		0.1	1.5	µA
TURN-OFF/-ON SPECIFICATIONS						
Burst-Enable Time		(Notes 2, 6, 7)			2.3	ns
Burst-Disable Time		(Notes 2, 6, 8)			2.0	ns

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, I_{BIAS} = 20mA, I_{MOD} = 30mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SAMPLE/HOLD SPECIFICATIONS						
MDIN Voltage Range			0.05		2.56	V
MDOUT Settling		Relative to final value at 3µs, C_L < 20pF			±1	mV
Sample/Hold Droop		After 100µs (Note 9)			±2.56	mV
Sampling Error		Final value measured after 10µs (MDOUT - MDIN), burst width > 576ns		3	±14	mV
BANDGAP VOLTAGE REFERENCE SPECIFICATIONS						
VREF Output		R_L > 10kΩ, C_L < 50pF	1.175	1.235	1.295	V
MODULATION/BIAS CURRENT DISABLE						
Enable Time		5mA < I_{BIAS}, 10mA < I_{MOD} (Note 10)			5.5	µs
Disable Time		(Notes 2, 11)			375	ns
R_{IMAX} Range			3		15	kΩ
Current Limit (Tested with I_{BIAS} = I_{MOD})	I_{BIAS}+I_{MOD}	R_{IMAX} = 3kΩ	155			mA
		R_{IMAX} = 5kΩ	100		150	
		R_{IMAX} = 10kΩ	50		75	
OPTICAL EVALUATION						
Eye Margin		1.25Gbps (Note 12)		33		%

Note 1: DC parameters are production tested at T_A = +25°C, guaranteed by design and characterization at T_A = -40°C. AC parameters are guaranteed by design and characterization.

Note 2: For 10mA ≤ I_{MOD} ≤ 85mA and 4mA ≤ I_{BIAS} ≤ 70mA.

Note 3: Deterministic jitter measured with a continuous pattern of 2^7-1 PRBS, 80 ones, 2^7-1 PRBS, 80 zeros at 1.25Gbps, and both LVPECL inputs terminated by the network shown in Figure 3.

Note 4: Random jitter, rise time, fall time measured with 0000011111 pattern at 1.25Gbps.

Note 5: Voltage difference between VMSET and MODSET or VBSET and BIASSET excluding IR drops. The maximum operating voltage at VMSET or VBSET must be less than 1.4V for proper operation.

Note 6: Turn-on/-off time is when the BEN+/BEN- LVPECL inputs are used to control modulation and bias currents.

Note 7: Burst-enable delay is measured between the time at which the rising edge of the differential burst-enable input reaches the midpoint, and the time at which the combined output currents (bias plus modulation) reach 90% of their final level.

Note 8: Burst-disable delay is measured between the time at which the falling edge of the differential burst-enable input reaches the midpoint, and the time at which the combined output currents (bias plus modulation) fall below 10% of the bias-on current.

Note 9: Droop measured with sample/hold output load of 10MΩ.

Note 10: Enable delay is measured between the time at which the falling edge of the $\overline{EN}$ input reaches ≤ 0.8V, and the time at which the combined output currents (bias plus modulation) reach 90% of their final level.

Note 11: Disable delay is measured between the time at which the rising edge of the $\overline{EN}$ input reaches ≥ 2V, and the time at which the combined output currents (bias plus modulation) fall below 10% of the bias-on current.

Note 12: Excelight SXT5731-Q laser.

Note 13: Current gain stability = [(Gain – nominal Gain) / nominal Gain], nominal Gain at V_{CC} = 3.3V, T_A = +25°C.

Note 14: Gain linearity = $\frac{(Gainmax - Gainmin)}{Gainavg/2}$, Gainavg = $\frac{Gainmax - Gainmin}{2}$

Note 15: Gain matching = $\left| \frac{Gainmod / Gainbias - Gainmodnom / Gainbiasnom}{Gainmodnom / Gainbiasnom} \right|$ nominal at V_{CC} = 3.3V, T_A = +25°C.

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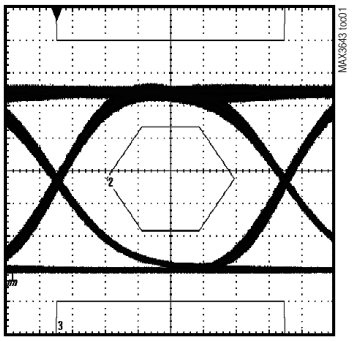
Typical Operating Characteristics

(Typical values are at V_{CC} = +3.3V, T_A = +25°C, data pattern = 2^7-1 PRBS + 80 ones + 2^7-1 PRBS + 80 zeros, unless otherwise noted.)

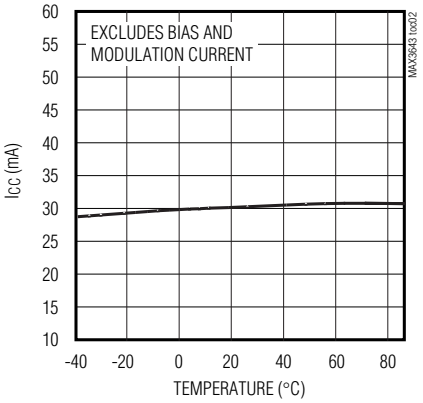
OPTICAL EYE DIAGRAM (1.25Gbps, 933MHz FILTER, PATTERN 2^{13}-1 + 80 CID)



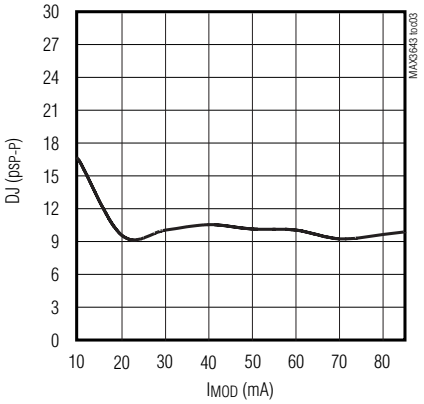
EXCELIGHT SXT5731-Q LASER

AVERAGE OPTICAL POWER = 3dBm
EXTINCTION RATIO = 15dB
GbE MASK MARGIN = 33%

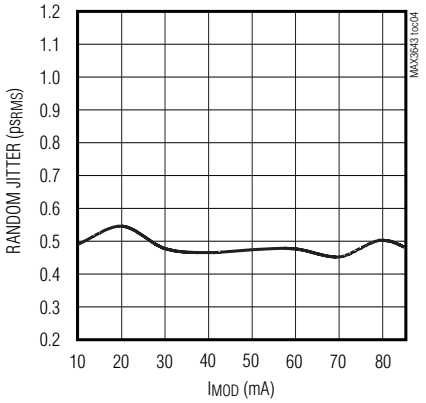
SUPPLY CURRENT vs. TEMPERATURE (I_{BIAS} = 20mA, I_{MOD} = 30mA)



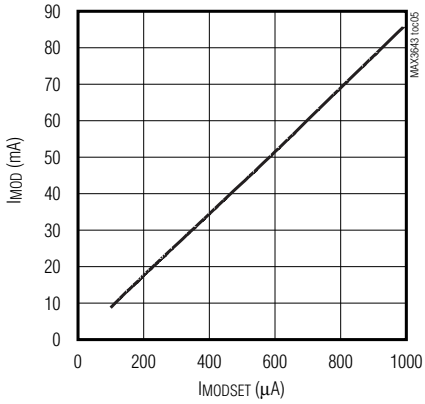
DETERMINISTIC JITTER vs. MODULATION AMPLITUDE



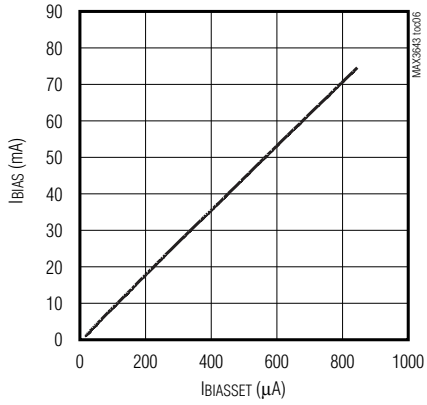
RANDOM JITTER vs. MODULATION AMPLITUDE



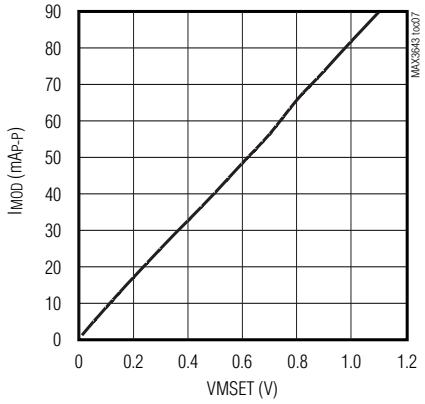
IMOD vs. IMODSET



IBIAS vs. IBIASSET



IMOD vs. VMSET (R_{MODSET} = 1kΩ)

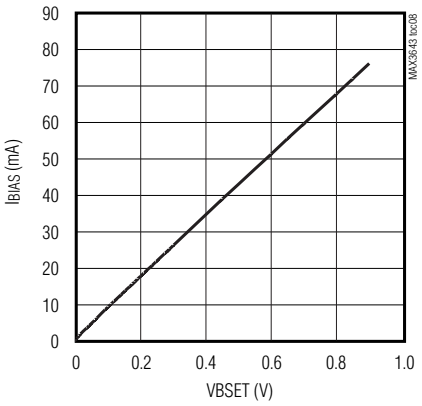


155Mbps to 2.5Gbps Burst-Mode Laser Driver

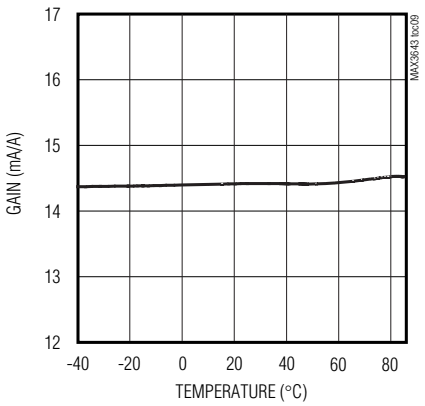
Typical Operating Characteristics (continued)

(Typical values are at V_{CC} = +3.3V, T_A = +25°C, data pattern = 2^7-1 PRBS + 80 ones + 2^7-1 PRBS + 80 zeros, unless otherwise noted.)

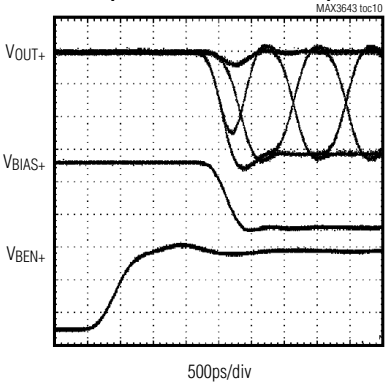
IBIAS vs. VBSET (RBIASSET = 1kΩ)



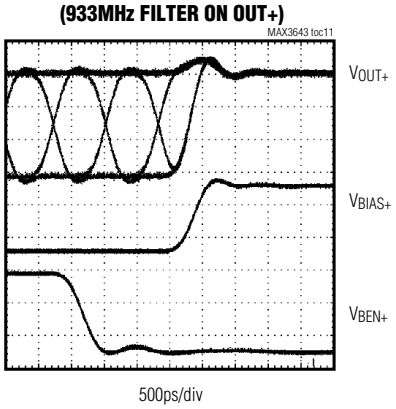
BIAS CURRENT MONITOR GAIN (IBCMON/IBIAS) vs. TEMPERATURE



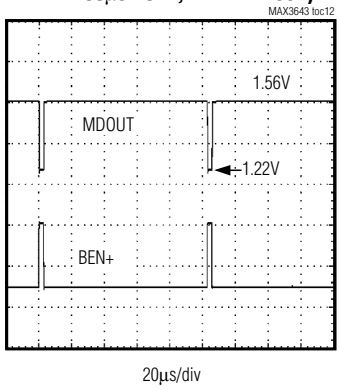
TIMING DIAGRAM, BURST-ON (933MHz FILTER ON OUT+)



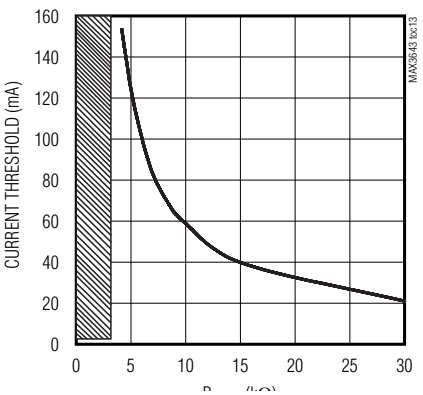
TIMING DIAGRAM, BURST-OFF (933MHz FILTER ON OUT+)



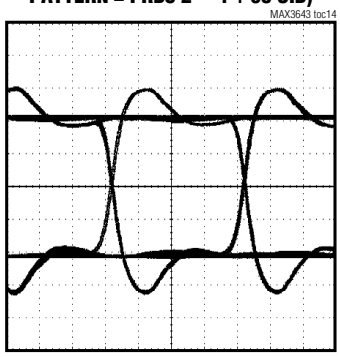
SAMPLE/HOLD (10MΩ LOAD, 2.8µs SAMPLE AND 100µs HOLD, MDIN = 1.56V)



IBIAS + IMOD CURRENT THRESHOLD vs. RIMAX



ELECTRICAL EYE DIAGRAM (2.5Gbps, IMOD = 30mA, PATTERN = PRBS 2^7 - 1 + 80 CID)



Pin Description

PIN	NAME	FUNCTION
1	V_{CCA}	Analog Supply Voltage
2	IN+	Noninverted Data Input, LVPECL Compatible
3	IN-	Inverted Data Input, LVPECL Compatible
4	V_{CCS}	Signal Supply Voltage
5	BEN+	Noninverted Burst-Enable Input, LVPECL Compatible
6	BEN-	Inverted Burst-Enable Input, LVPECL Compatible
7	BENOUT	Burst-Enable Output, LVCMOS. Signal replicates BEN input.
8	$\overline{EN}$	Enable Input LVCMOS. Active low enables BIAS± and MOD± outputs.
9	BCMON	Bias Current Monitor. Current out of this pin develops a ground-referenced voltage across an external resistor proportional to the bias current.
10	IMAX	Current-Limit Reference. Connect a resistor from IMAX to GND to set maximum I_{BIAS} plus I_{MOD}.
11	MDOUT	Monitor Diode Out. Analog Output for sample/hold.
12	MDIN	Monitor Diode In. Analog Input for sample/hold.
13	BIAS-	Connect BIAS- to V_{CC} Through a 15Ω Resistor (or 5Ω Resistor and Switching Diode)
14	BIAS+	Laser Bias Current Output. Modulation current flows into this pin when BEN input is high.
15, 18	V_{CCO}	Output Supply Voltage
16	OUT+	Laser Modulation Current Output. Modulation current flows into this pin when both BEN and IN inputs are high.
17	OUT-	Connect OUT- to V_{CC} Through a 15Ω Resistor (or 5Ω Resistor and Switching Diode)
19	GND	Supply Ground. This pin must be connected to ground.
20	MODSET	Modulation Current Set. Current from this pin to ground sets the laser modulation current.
21	VMSET	MODSET Reference. A ground-referenced voltage at this point establishes the MODSET reference.
22	VREF	Reference Voltage Output. May be used for VMSET, VBSET.
23	VBSET	BIASSET Reference. A ground-referenced voltage at this point establishes the BIASSET reference.
24	BIASSET	Bias Current Set. Current from this pin to ground sets the laser bias current.
EP	EP	Exposed Paddle (Ground). The exposed pad must be soldered to the circuit board ground for proper thermal and electrical operation.

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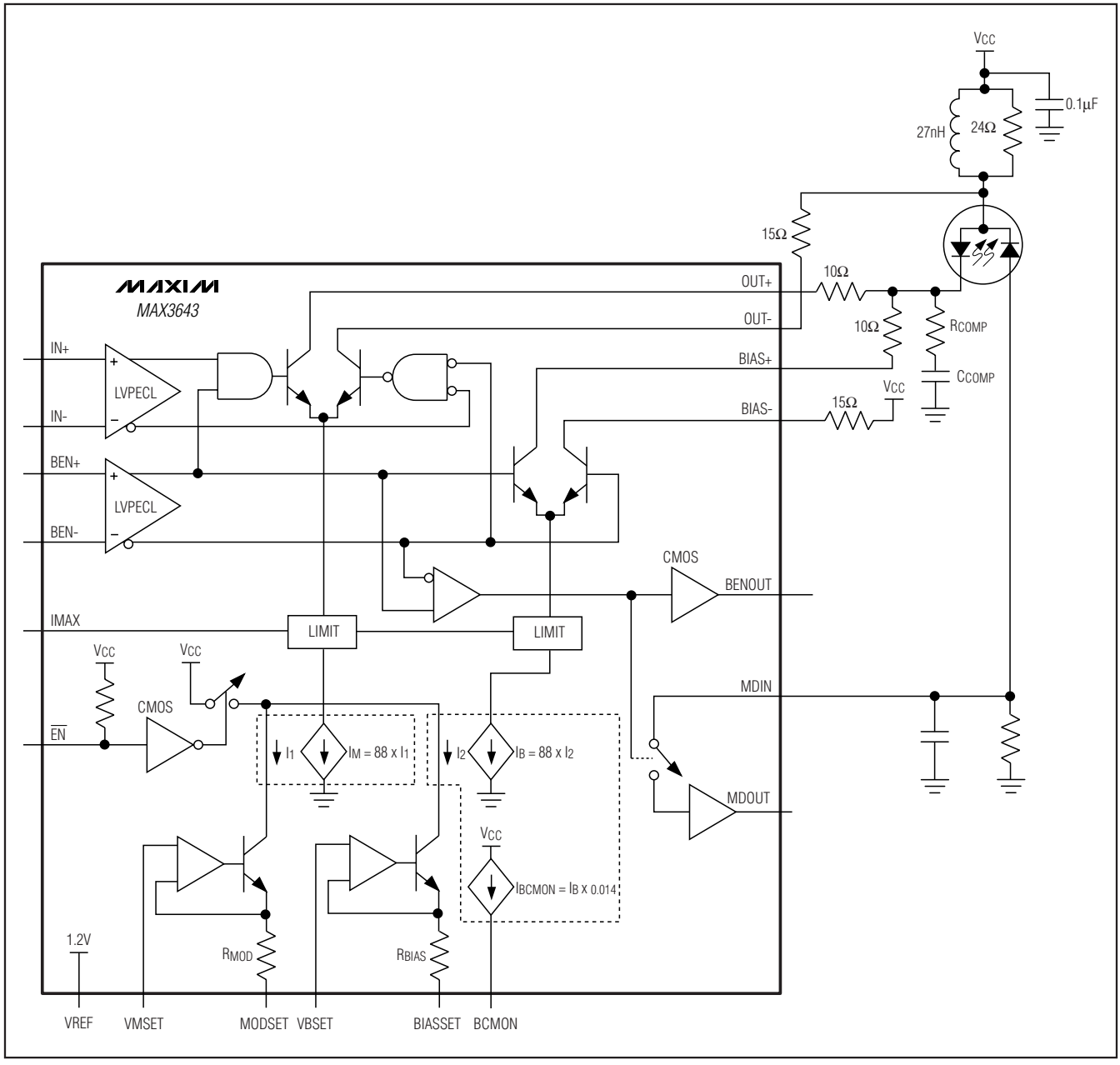

Figure 1. Functional Diagram

Detailed Description

The MAX3643 laser driver includes a bias current generator, bias current monitor, modulation current generator, laser drive outputs, and monitor diode sample and hold. LVPECL-compatible inputs are provided for both high-speed data and burst enable. The high-speed burst-enable input signal is replicated on an LVCMOS output for use by the controller.

Laser Diode Modulation and Bias Current Generators

Laser diode modulation current amplitude is controlled by the current out of the MODSET pin, and bias current by the current out of the BIASSET pin, according to:

$$I_{MOD} = I_{MODSET} \times 88$$
$$I_{BIAS} = I_{BIASSET} \times 88$$

A voltage source and two op amps are provided to enable I_{MODSET} and $I_{BIASSET}$ to be set using either a resistor to ground or a current digital-to-analog converter (DAC). The high-impedance op amp reference input can be externally controlled, so that the modulation and bias currents can also be set using voltage DACs.

Laser Diode Modulation and Bias Current Limiter

Typical laser diodes have an absolute maximum rating of 150mA. To reduce the possibility of laser damage, the modulation current and bias current are shut off if the sum I_{MOD} + I_{BIAS} attempts to exceed the limit set by R_{IMAX}; see the *Typical Operating Characteristics*.

Bias Current Monitor

The laser diode bias current can be monitored by measuring the voltage across an external load resistor connected from BCMON to ground. For example, a 1kΩ resistor from BCMON to ground gives the following relationship:

$$V_{BCMON} = I_{BIAS} \times G_{BSM} \times 1k\Omega$$

The voltage at BCMON must be below 1.4V for proper operation.

Output Drivers

The modulation current ranges from 10mA to 85mA, as set by the current through MODSET. The laser modulation current output OUT+ is optimized to drive a 15Ω load, and must be DC-coupled. A damping resistor, R_D, provides impedance matching to the laser diode. The combined value of the series damping resistor and the laser diode equivalent series resistance should be close to 15Ω. An RC shunt network, R_{COMP}/C_{COMP}, should also be provided to reduce optical output aberrations and duty-cycle distortion. The values of R_{COMP} and C_{COMP} can be adjusted to match the laser and PC board layout characteristics for optimal optical eye performance. The OUT- pin is normally connected through a 15Ω resistor to V_{CC} or through a switching diode and series resistor to V_{CC}. With some laser diodes, the use of a switching diode at OUT can improve the optical output eye by better matching the laser characteristics.

The bias current ranges from 1mA to 70mA, as set by the current through BIASSET. Current in the BIAS output also switches at high speed when bursting; therefore, the BIAS+ pin should be connected directly through a resistor, equal to R_D as determined above, to the laser cathode. The BIAS- pin must also be connected through a 15Ω resistor or through a switching diode and series resistor to V_{CC}.

When the BEN input is high, the laser driver sinks bias and modulation current according to the settings at MODSET and BIASSET. When the BEN input is low, the BIAS+ and OUT+ currents both shut off within 2ns. Note that when BEN is low, the bias current is shunted through the BIAS- output and the modulation current through the OUT- output.

Monitor Diode Sample and Hold

Laser monitor diode current is only generated when there is an optical output (BEN is active). When BEN is inactive, the monitor current is zero, reflecting the fact that the laser is off. A sample-and-hold circuit, triggered by the state of the BEN input, is provided in the MAX3643. During the burst-enable active period, the voltage present at MDIN is stored on an internal sample-and-hold capacitor; and during the burst-enable inactive period, that voltage is output on MDOUT; see the timing diagram in Figure 2.

While the internal sample-and-hold is sampling (BEN active), MDOUT voltage takes a 1.2V reference level.

155Mbps to 2.5Gbps Burst-Mode Laser Driver

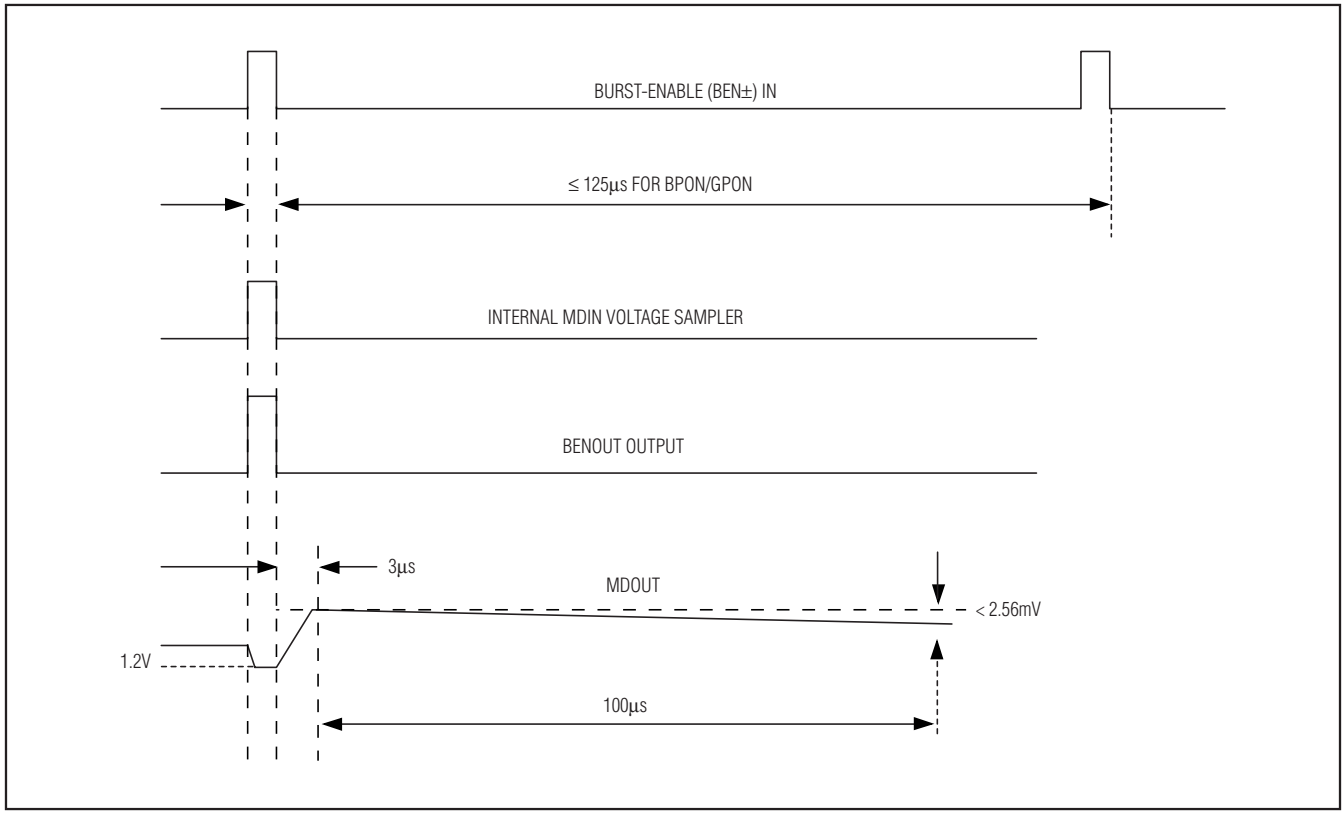

Figure 2. Sample-and-Hold Timing Diagram

Enable Input

An LVCMOS input, $\overline{EN}$, is provided to disable both bias and modulation currents under external control. The maximum time to disable laser current with the $\overline{EN}$ control is 375ns.

Setting the Current Limit

A current limiter is provided to protect the laser diode by shutting down both bias and modulation currents when total current exceeds a value set by the resistor connected from IMAX to ground. Do not use less than 3kΩ I_{MAX}. See the I_{BIAS} + I_{MOD} Current Threshold vs. R_{IMAX} graph in the *Typical Operating Characteristics.*

Programming the MODSET and BIASSET Inputs

To program the laser modulation current using a current DAC, connect VMSET to VREF, attach the DAC to the MODSET pin and set the current according to:

$$I_{MOD} = I_{MODSET} \times 88$$

To program the laser modulation current using a resistor or digital potentiometer, connect VMSET to VREF, attach a resistor from the MODSET pin to ground, and set the current according to:

$$I_{MOD} = \frac{1.2V}{R_{MODSET} + R_{MOD}} \times 88$$

To program the laser modulation current using a PWM voltage DAC (requiring a high-impedance load), attach a DAC output to the VMSET pin, connect a resistor from the MODSET pin to ground as shown in the *Typical Applications Circuit*, and set the current according to:

$$I_{MOD} = \frac{V_{DAC}}{R_{MODSET} + R_{MOD}} \times 88$$

This approach can also be used for a conventional voltage DAC output, if desired. In all cases, the voltage at MODSET must be kept ≤ 1.4V, which limits the range of acceptable values for R_{MODSET} depending on the maximum modulation current.

Laser diode bias current is set in the same manner as modulation current.

LVPECL Data/Burst-Enable Inputs

The MAX3643 data and BEN inputs are biased with an on-chip, high-impedance network. When DC-coupled, the MAX3643 operates properly with signals that meet the EC table input-swing and common-mode requirements, including LVPECL and most CML.

See Figure 3 for a termination network that can be used to connect the data and BEN inputs to LVPECL data outputs. Other termination networks may also be used, as long as both the input swing and common limits are met.

Sample-and-Hold Operation

When the MAX3643 internal sample-and-hold is not required, the MDIN pin should be connected to ground and the MDOUT pin unconnected. If the internal sample-and-hold is required, then it is necessary to ensure that the time constant resulting from the monitor diode load resistance and the total load capacitance is compatible with the desired minimum burst interval. It is also necessary to make certain that the load at MDOUT does not exceed the capability of the MDOUT pin.

Because the voltage at MDIN is not reflected to MDOUT until after the end of the laser burst, systems using the internal sample-and-hold alone cannot support continuous mode operation, often a required feature for module calibration. In this case, the voltage at MDIN can also be connected directly to a mux input as shown in the *Typical Applications Circuit*. As long as the total capacitance (including monitor diode intrinsic capacitance, MDIN capacitance, mux off-capacitance, and wiring parasitics) is less than 50pF, and the monitor diode load resistor is less than 2kΩ, then the sample-and-hold captures a 576ns minimum burst. The MAX3643 typical MDIN capacitance is 5pF, typical monitor diode maximum capacitance is 25pF, and the typical capacitance of a mux input in the off-state is 3pF to 5pF. When the mux is in the on-state, the capacitance at the input is typically 10pF to 20pF.

If the minimum burst duration is longer than 576ns, it may be useful to connect an external capacitor in parallel with the monitor diode load to limit the effects of the data pattern on the monitor diode output.

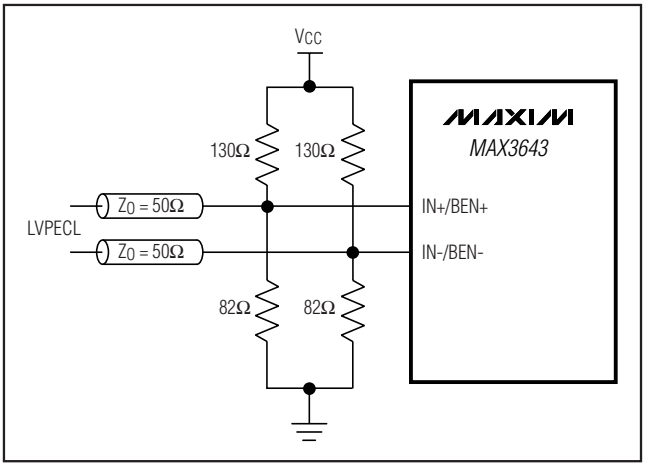

Figure 3. LVPECL High-Speed Inputs

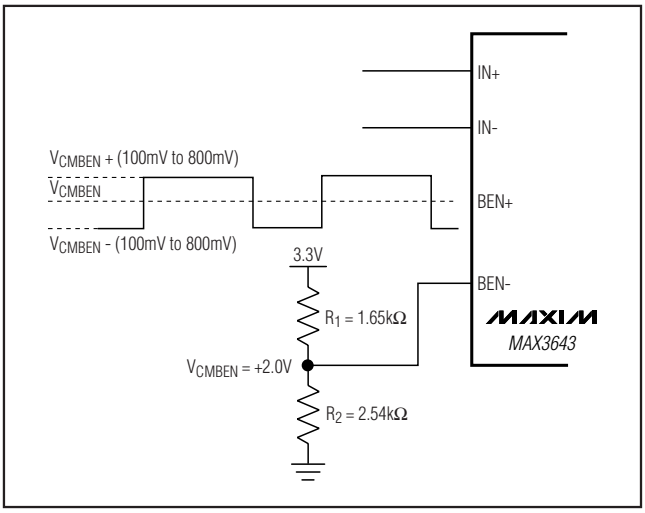

Figure 4. Single-Ended Biasing for Burst Enable

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Applications Information

Running Burst-Enable Single-Ended

See Figure 5 for setting up the single-ended LVTTL or LVCMOS biasing for burst enable.

Layout Considerations

To minimize inductance, keep the connections between the MAX3643 output pins and laser diode as close as possible. Optimize the laser diode performance by placing a bypass capacitor as close as possible to the laser anode. Take extra care to minimize stray parasitic capacitance on the BIAS and MD pins. Use good high-frequency layout techniques and multilayer boards with uninterrupted ground planes to minimize EMI and crosstalk.

Laser Safety and IEC 825

Using the MAX3643 laser driver alone does not ensure that a transmitter design is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Each user must determine the level of fault tolerance required by the application, recognizing that Maxim products are neither designed nor authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application in which the failure of a Maxim product could create a situation where personal injury or death can occur.

Exposed-Paddle Package

The exposed paddle on the 24-pin TQFN provides a very low thermal resistance path for heat removal from the IC. The pad is also electrical ground on the MAX3643 and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Maxim Application Note *HFAN-08.1: Thermal Considerations for QFN and Other Exposed-Paddle Packages* for additional information.

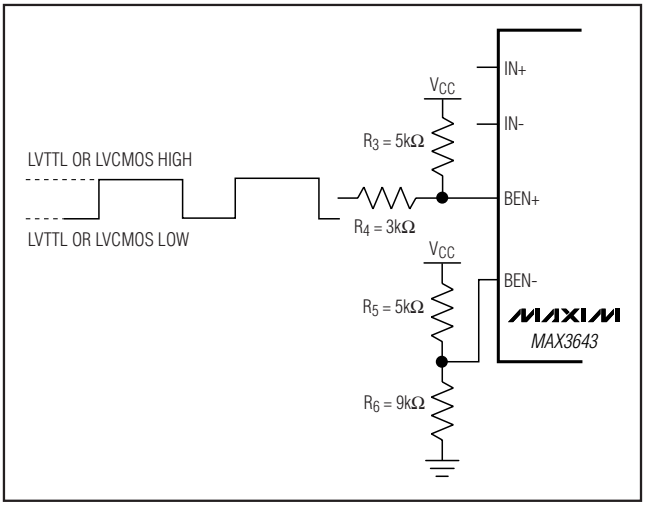

Figure 5. Single-Ended LVCMOS or LVTTL Biasing for Burst Enable

Interface Model

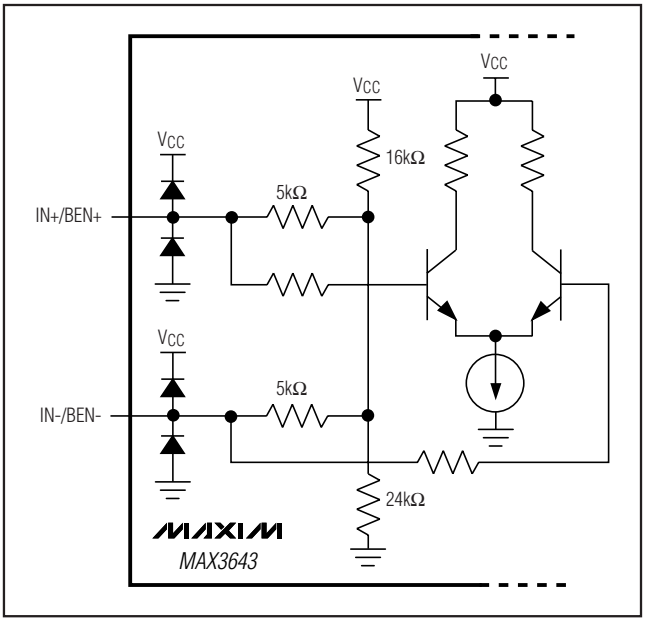

Figure 6. Simplified Input Circuit Schematic

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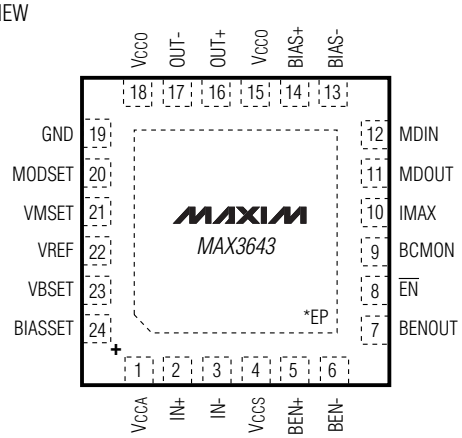
Pin Configuration



THIN QFN (4mm x 4mm)

*THE EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER THERMAL AND ELECTRICAL PERFORMANCE.

Chip Information

TRANSISTOR COUNT: 2771

PROCESS: SiGe BiPOLAR

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
24 TQFN-EP	T2444-3	**21-0139**

155Mbps to 2.5Gbps Burst-Mode Laser Driver

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/05	Initial release.	—
1	10/08	Added “155Mbps to 2.5Gbps” to the data sheet/part title.	All
		Updated the *Applications* section.	1
		In the *Operating Conditions* table, changed the data rate from 1250Mbps to 2500Mbps.	2
		In the *Typical Operating Characteristics*, added the ELECTRICAL EYE DIAGRAM graph.	6